In the Specification:

Add the following paragraphs:

BRIEF DESCRIPTION OF THE DRAWINGS

[0012.1] FIG. 1 is a block diagram of a known electrical circuit having three memories.

[0012.2] FIG. 2 is a block diagram of one memory part of FIG. 1.

[0012.3] FIG. 3 is a block diagram of a circuit having a 3-bit scan path.

[0012.4] FIGS. 4A and 4B are block diagrams of a bypass memory of FIG. 3.

[0012.5] FIG. 5 is a block diagram of three circuits of FIG. 3 connected in series to a tester.

[0012.6] FIG. 6 is a block diagram of N circuits connected on a scan path in a known manner.

[0012.7] FIG. 7 is a block diagram of N circuits connected on a scan path according to the disclosed invention.

[0012.8] FIG. 8 is a block diagram of N circuits connected on a scan path and depicting N progressive scan test patterns.

[0012.9] FIG. 9 is a block diagram of a circuit similar to that in FIG. 3 with only a 2-bit scan path.

[0012.10] FIG. 10 is a block diagram of a circuit similar to that in FIG. 3 with a greater number of outputs than inputs.

[0012.11] FIG. 11 is a block diagram of a scan cell C of FIG. 10.

[0012.12] FIG. 12 is a block diagram of the circuit of FIG. 10 modified to accept the warping scan test concept.

[0012.13] FIG. 13 is a block diagram of a summing cell (DSC).

[0012.14] FIG. 14 is a block diagram of a scan testable circuit.

[0012.15] FIG. 15 is a block diagram of a data retaining cell (DRC).

[0012.16] FIG. 16 is a block diagram of an implementation of a warping scan test concept.

[0012.17] FIG. 17 is a block diagram of another implementation of a warping scan test concept.

[0012.18] FIG. 18 is a block diagram of another implementation of a warping scan test concept.

[0012.19] FIG. 19 is a block diagram of a data capture boundary cell (DCBC).

[0012.20] FIG. 20 is a block diagram of a data retaining boundary cell (DRBC).

[0012.21] FIG. 21 is a block diagram of a data summing boundary cell (DSBC).

[0012.22] FIG. 21A is a block diagram of a realization of DCBC, DRBC, and DSBC.

[0012.23] FIG. 22 is a block diagram of circuits Cl-CN being tested inside an IC or die.

[0012.24] FIG. 23 is a block diagram of ICs 1-N being tested on a circuit board.

[0012.25] FIG. 24 is a block diagram of boards BD being tested in a box.

[0012.26] FIG. 25 is a block diagram of multiple boxes 1-N being tested in a system.

[0012.27] FIG. 26 is a representation of dies being tested on a wafer.

[0012.28] FIG. 27 is a block diagram of a test access port on a die.

[0012.29] FIG. 28 is a representation of wafers, each carrying dies, being tested in a lot.

[0012.30] FIG. 29 is a representation of wafer lots 1-N beings tested.

[0012.31] FIG. 30 is a block diagram of a circuit and scan path with conventional signature analyzers.

[0012.32] FIG. 31 is a representation of a wafer with additional bussing and test pads.

[0012.33] FIG. 32 is a block diagram of a test access port on a die.

[0012.34] FIG. 33 is a block diagram of a conventional IEEE STD 1149.1 scan cell.

[0012.35] FIG. 34 is a block diagram of a circuit using four conventional scan cells S.

[0012.36] FIG. 35 is a block diagram of a circuit similar to that of FIG. 34.

[0012.37] FIG. 36 is a block diagram of a circuit relating to an input buffer.

[0012.38] FIG. 37 is a block diagram of a circuit relating to a bi-directional pad.

[0012.39] FIG. 38 is a block diagram of the circuits of FIGS. 34-37 bussed together on a die.

[0012.40] FIG. 39A is a block diagram of a 3-state output buffer.

[0012.41] FIG. 39B is a block diagram of a known ESD circuit.

[0012.42] FIG. 39C is a block diagram of another known ESD circuit.

[0012.43] FIG. 40A is a block diagram of a tester and an input buffer.

[0012.44] FIG. 40B is a block diagram of a known ESD circuit.

[0012.45] FIG. 41 is a block diagram of a tester and an analog output buffer.

[0012.46] FIG. 42 is a block diagram of a tester and an analog input buffer.